Electronic Version
Stylesheet Version v1.1.1

Description

COMPLIANT PASSIVATED EDGE SEAL FOR LOW-K INTERCONNECT STRUCTURES

BACKGROUND OF INVENTION

[0001] This invention relates generally to interconnect structures for high-speed microprocessors, application specific integrated circuits (ASICs), and other high speed ICs, and more specifically, to a compliant passivated edge seal for low-k interconnect structures. This invention provides computer chips with improved mechanical integrity in the assembly and packaging, and also provides many additional advantages which shall become apparent as described below.

[0002] In semiconductor fabrication, insulating, semiconducting, and conducting layers are formed on a substrate. The layers are patterned to create features and spaces, forming devices, such as transistors, capacitors and resistors. These devices are then interconnected to achieve a desired electrical function, thereby producing an integrated

circuit (IC). The formation and patterning of the various device layers are achieved using conventional fabrication techniques, such as oxidation, implantation, deposition, epitaxial growth of silicon, lithography, etching and planarization.

[0003] To increase throughput, a plurality of ICs are fabricated on a wafer in parallel. Thus, for example, a wafer may contain multiple IC units which have been formed on the planar surface area of the wafer. Each IC is a self contained entity surrounded by its own boundary region using orthogonal axes that are referred to as dicing channels or scribe lanes. Generally, these channels may have a width of about 50 to 100 μm. The ICs are typically separated into individual chips or "die" by cutting in this channel in a process known as "dicing" or "singulation". Conventional dicing techniques include sawing with a diamond wheel, laser cutting, and "scribe and break". As the dicing tool cuts or scribes the wafer, chips and cracks in the surface and substructure often result. Such cracks can propagate into critical areas within the IC in response to packaging stresses, and may cause permanent circuit failure.

[0004] To increase chip performance, wiring capacitance is re-

duced by changing from the industry-standard dielectric material SiO_2 (having a relative dielectric constant of about 4.0) to lower dielectric constant ("low-k") insulators surrounding the interconnects. These low-k materials come at a significant disadvantage of loss of mechanical properties such as hardness and elastic modulus, and other forms of robustness and resistance to failure due to internal and external stresses. In particular, it has become a problem to probe, dice, and package chips containing low-k insulators without causing fracture, chipping or cracking of the dielectric material, and pullout of the terminal metal pads. There is therefore a need to isolate these weak on-chip materials from the harsh external environment and stresses associated with assembly and packaging.

[0005] Typical prior art approaches have adopted a hard dielectric passivation layer such as a silicon nitride material. For example, U.S. Patent No. 5,742,094 discloses a sealed semiconductor chip. A hermetic seal consisting of a thin SiN passivation layer and a Ni passivation layer is selectively deposited on the chip surface. It has been observed, however, that when a low-k dielectric material is used as the inter-metal dielectric within the active area of the

chip, such hard passivation layers do not adequately protect the device from fracture, chipping or cracking of the dielectric material, and pullout of the terminal metal pads.

[0006] Other prior art approaches combine a hard dielectric passivation layer such as a silicon dioxide or silicon nitride with an overcoat of a more compliant material such as a polyimide. For example, U.S. Patent No. 6,383,893 discloses a hard passivation layer (124) consisting of inorganic insulators such as SiO_2 or SiN covering the wafer, and a soft passivation layer (125) consisting of polyimide overlying the hard passivation layer. U.S. Patent No. 6,271,578 discloses a similar structure. Again, it has been observed that when a low-k dielectric material is used as the inter-metal dielectric within the active area of the chip, a hard passivation layer in contact with the active device area does not adequately protect the device from fracture, chipping or cracking of the dielectric material, and pullout of the terminal metal pads. The soft passivation layer overlying the hard passivation layer fails to alleviate this problem.

[0007] Another prior art approach disclosed in U.S. Patent No. 5,665,655 involves the use of a crackstop structure, specifically a groove surrounding the active region on a

chip. In this structure, a dielectric material (3) which can be polyimide is deposited over the substrate including the active device regions, and then a hard passivation layer (11) of, for example, silicon nitride is deposited over the structure. When the dicing operation is performed, however, the sidewalls of the chip remain in contact with the substrate material, which is typically a semiconductor material such as silicon. Microcracks occurring in silicon substrates tend to propagate very rapidly, and would therefore lead to failures in the adjacent low-k dielectric material. Thus, this structure also fails to protect the device from fracture, chipping or cracking of the dielectric material, and pullout of the terminal metal pads.

[0008] Therefore, a need remains in the art for a structure and process to isolate the weak on-chip materials from the harsh external environment and stresses associated with assembly and packaging.

SUMMARY OF INVENTION

[0009] The aforementioned problems are addressed by the structure and method of this invention. Specifically, in one aspect this invention is directed to a semiconductor wafer comprising a substrate; a plurality of integrated circuits fabricated on the substrate; a dicing channel disposed be-

tween adjacent ones of the integrated circuits, the channel exposing sidewalls of the integrated circuits; a layer of first dielectric material disposed on a top surface and sidewalls of the integrated circuits; and a layer of second dielectric material disposed on the layer of first dielectric material, wherein the first dielectric material has a critical strain energy release rate, G_c at least about 10 times greater than the second dielectric material. The first dielectric material preferably also has a tensile strength of about 20 to 100 MPa.

[0010] In another aspect, this invention is directed to a method of forming an edge seal structure on an integrated circuit chip formed on a substrate. The method comprises: etching a channel in a kerf region surrounding the integrated circuit chip, thereby exposing sidewalls of the integrated circuit chip; depositing a planarizing layer of first dielectric material on the integrated circuit chip and in the channel; and depositing a second dielectric material over the first dielectric material, wherein the first dielectric material has a G_c value at least about 10 times greater than the second dielectric material.

BRIEF DESCRIPTION OF DRAWINGS

[0011] The features of the invention believed to be novel and the

elements characteristic of the invention are set forth with particularity in the appended claims. The drawings are for illustration purposes only and are not drawn to scale. Furthermore, like numbers represent like features in the drawings. The invention itself, however, both as to organization and method of operation, may best be understood by reference to the detailed description which follows, taken in conjunction with the accompanying drawings, in which:

[0012] Figure 1 illustrates an embodiment of the present invention in which final passivation and compliant layers terminate perpendicular to and onto the substrate; and

[0013] Figure 2 illustrates another embodiment of the present invention in which the compliant layer terminates perpendicular to and onto the substrate, and the final passivation layer terminates adjacent to a previously diced substrate.

DETAILED DESCRIPTION

[0014] The invention involves a structure and method to generate a mechanical isolation region between the final on-chip interconnect level and the terminal pads and dicing channel of the chip, while still providing electrical continuity through this region via flexible connections. The isolation material and flexible electrical feed-throughs allow for

strain relief and shock absorption without permanent damage to the chip wiring levels.

[0015] Figure 1 illustrates one embodiment of the invention. In the structure shown in Figure 1, integrated circuit (IC) 11 has been formed on substrate 10. IC 11 comprises the active device regions of the chip (not shown), interconnect wiring 12, and metal pads 13. Surrounding the IC is a layer 16 of energy absorbing material which is capable of absorbing mechanical stresses imparted onto the IC 11 during assembly and packaging. A final passivation layer 17 is disposed over the layer 16 to hermetically seal the chip prior to dicing. Embedded in layer 16 are a plurality of conductive leads 14 connecting the metal pads 13 with bonding pads 15. Leads 14 may be jogged or staggered, as shown, or they may be straight. The energy absorbing material 16 contacts the sides of IC 11, in addition to the top surface of IC 11.

[0016] The energy absorbing layer 16 and the final passivation layer 17 should each be passivated, i.e., formed of dielectric material. In addition, the energy absorbing material 16 should be compliant yet tough. This material may be characterized by fracture toughness, which may be defined as a material's ability to resist the propagation of a

crack within itself. The parameter G_c is known as the critical strain energy release rate, or the energy at which a crack will propagate. G_c has units of kJ/m^2, and is often referred to as the fracture toughness of a material. Another parameter that is frequently encountered when quantifying the fracture toughness of a material is the critical stress intensity factor, K_c. The relationship between G_c and K_c is as follows: $G_c = K_c^2/E$ for plane stress and $G_c = K_c^2(1-\nu^2)/E$ for plane strain, where ν is Poisson's ratio. K_c has units of $MPa\text{-}m^{1/2}$. Low values of G_c and K_c are indicative of low fracture toughness. Materials having low fracture toughness typically will exhibit brittle failure. High values of G_c and K_c are indicative of high fracture toughness, where failure modes are likely to be ductile.

[0017] One may record the stress-strain curve for a given set of materials in a static tensile test at constant temperature and strain rate as performed in accordance with ASTM methods. Those materials that exhibit low fracture toughness typically exhibit brittle failure and will fail at very low strains in the region of 1-3%. Those materials that exhibit some degree of yield or elongation to break will fail at high strains >10% and are typical of materials with high fracture toughness and ductile failure modes. Thus, the

energy absorbing material 16 preferably has a fracture toughness which is at least about 10 times greater than the fracture toughness of the final passivation layer 17. The energy absorbing material 16 preferably has a G_c greater than about 0.1 kJ/m^2, and more preferably in the range of about 0.5 to 2.5 kJ/m^2. The final passivation layer 17 preferably has a G_c less than about 0.05 kJ/m^2, and more preferably in the range of about 0.005 to 0.05 kJ/m^2.

[0018] The energy absorbing material 16 also may be characterized by tensile strength. The tensile strength or ultimate tensile strength of a material may be defined as the maximum stress the material under load can attain prior to failure. Tensile strength is typically expressed in units of MPa (MN/m^2). One may record the stress-strain curve in a static tensile test at constant temperature and strain rate as performed in accordance with ASTM methods, and from this plot mark the tensile strength as previously defined. Those materials that exhibit low tensile strength typically experience brittle failure and will fail at very low strains in the region of 1-3%. Those materials that exhibit some degree of yield or elongation to break will fail at high strains >10% and typically have high tensile strength and ductile

failure modes. The yield stress, σ_y, may be reported to indicate a material's strength and is a very different point on the stress-strain curve. Some materials yield or "neck down" when under load; this is exhibited as a maximum in the stress-strain curve followed by a slight drop in stress for constant strain. The material may then continue to carry load with only a gradual increase in stress with increase in strain (known as elongation) until failure occurs. The energy absorbing material 16 preferably has a tensile strength of about 20 to 100 MPa, while the final passivation layer 17 preferably has a tensile strength of about 700 to 10,000 MPa.

[0019] Any material exhibiting the above described characteristics may be used for the energy absorbing material 16. Preferred materials are largely organic in nature, and include: polyesters, phenolics, polyimides, polysulfones, polyether ether ketones, polyurethanes, epoxies, polyarylene ethers, polyethylene terepthalates. For example, polystyrene has a G_c value of 1-2 kJ/m^2, and a tensile strength of 0.08 GPa. Other examples include polymethyl methacrylate with a G_c value of 0.2-0.6 kJ/m^2 and a K_c of 1.5 $MPa\text{-}m^{1/2}$, and polyethylene with tensile strength of 0.05 GPa. A particularly preferred energy absorbing mate-

rial is polyarylene ether known as SiLK™, available from Dow Chemical, and having a fracture toughness, K_c, of 0.62 MPa-$m^{1/2}$. An additional benefit of SiLK and some of the polyimides is thermal stability to relatively high temperatures such as from 350C to 450C; these materials would survive all subsequent processing involved in the chip fabrication or packaging.

[0020] The final passivation layer 17 may be formed of any material exhibiting the above described characteristics. Preferred materials are largely inorganic in nature, and include: silicon-based glasses such as SiN and SiO_2, SiC, tetraethylorthosilicate (TEOS), fluorinated TEOS (FTEOS), fluorinated silicate glass (FSG), and organosilicate glass (OSG). A particularly preferred material for the final passivation layer is SiO_2, having a tensile strength of 5900 MPa.

[0021] One skilled in the art will recognize that the energy-absorbing material and final passivation layer may be characterized by other material properties such as Young's modulus and hardness. Preferred materials for the final passivation layer include Si_3N_4, with modulus ranging from about 174 GPa to about 290 GPa and hardness of about 13.5 GPa; PECVD silane oxide with modulus of about 60 GPa and hardness of about 6.8 GPa; and fused

silica with modulus of about 72 GPa and hardness of about 8.7 GPa. The energy-absorbing material should generally have modulus and hardness values approximately two orders of magnitude lower than those for the final passivation layer. For example, SiLK™ has a modulus of about 3.5 GPa and hardness of about 0.21 GPa.

[0022] The structure shown in Figure 1 may be formed by the following method. A wafer comprising a plurality of ICs 11 is completed through processing of the final metal level, for example by copper/low-k dual damascene processing. The final metal level includes metal pads 13 to connect subsequently to terminal pads 15 for wirebond, C4 or direct pin creation.

[0023] Next, a channel is defined by conventional techniques, such as by photolithography, and is etched in the kerf region surrounding each chip 11. The channel is etched through the various layers residing on substrate 10, but is not etched through substrate 10. A planarizing layer of energy-absorbing material 16 is deposited, preferably spun on and cured, so as to fill the etched channels and to provide a planarized layer of this material over all active chip areas 11. Material layer 16 preferably has a thickness of about 1 to about 5 μm.

[0024] Contact holes are then created in the material layer 16 down to the metal pads 13. These holes may be created, for example, by photolithography and etching. Alternatively, if the material 16 is a photosensitive polyimide, then these holes may be directly patterned and etched. S-shaped or spring-shaped compliant leads 14 may be created which make contact with the exposed metal pads and rise up the side of the tapered holes in the material 15. For example, leads 14 may be created using the techniques disclosed by Hollie A. Reed et al. in "Compliant wafer level package (CWLP) with embedded air-gaps for sea of leads (SoL) interconnections," Proc. of IEEE 2001 IITC, pp. 151-153, the disclosure of which is incorporated herein by reference. As another example, leads 14 may be formed using the techniques disclosed by Khandros et al. in U.S. Patent No. 6,372,527 or U.S. Patent No. 6,538,214 or U.S. Patent No. 5,679,977, the disclosures of which are incorporated herein by reference.

[0025] Formation of leads 14 include the steps of sputtering a release layer and seed layer in the contact holes, forming a photomask over the material 16, through-mask plating of the compliant leads 14, removing the resist, and stripping the exposed seed layer and release layer. Optionally,

a second polymer layer (not shown) may be reflowed into the contact holes to plug the holes around the compliant leads. Leads 14 may be formed of any suitable metal, such as copper, aluminum, or tungsten.

[0026] Jogged leads 14 must be fabricated in two sequential stages. After the material 16 has been deposited, a suitable hardmask scheme may be employed to enhance the lithography of the via level of the jogged leads 14. The via level is defined using conventional lithography and etching techniques, followed by metallization and cap deposition. A second deposition of material 16 then may be applied and the line level of the jogged leads 14 may be defined using similar techniques, with an engineered offset as shown in Figure 1.

[0027] Next, the final passivation layer 17 is deposited. Layer 17 may comprise, for example, about 0.5 μm each of SiO_2 and Si_3N_4. Contact holes for terminal pads 15 are then formed using, for example, photolithography and etching. Metallurgy for terminal pads 15 is deposited in the contact holes, contacting the compliant leads 14 and plugging the contact holes through the final passivation layer 17. The wafer may then be diced and the individual chips may be packaged according to conventional processes.

[0028] In the structure of Figure 1, the hard passivation layer 17 is terminated on the substrate 10, forming a hermetic seal on the top surface of the substrate. Figure 2 differs from Figure 1 in that the hard passivation layer 17 forms an edge seal such that it encapsulates the entire substrate 10. The structure of Figure 2 may be formed by a method similar to the method for forming the structure of Figure 1, except that the channel must be etched at least partially through substrate 10, thereby exposing sidewalls of the substrate.

[0029] The structure and method of this invention may be used not only for die isolation, but also may be used for isolation of different macros on a die. The structure and method of this invention also may be used on the package rather than on the chip, providing similar mechanical isolation function.

[0030] While the present invention has been particularly described in conjunction with a specific preferred embodiment and other alternative embodiments, it is evident that numerous alternatives, modifications and variations will be apparent to those skilled in the art in light of the foregoing description. It is therefore intended that the appended claims embrace all such alternatives, modifica-

tions and variations as falling within the true scope and spirit of the present invention.